

JFW



Patent Application

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS: Allen et al. DOCKET: YOR920030406US1 (8728-649)
SERIAL NO: 10/733,210 GROUP ART UNIT: 2825
FILED: December 10, 2003 EXAMINER: Dinh, Paul
FOR: **FRAMEWORK FOR HIERARCHICAL VLSI DESIGN**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO RESTRICTION REQUIREMENT

Examiner:

In response to the Office Action dated January 6, 2005. Applicants provisionally elect the claims directed towards Group I (claim nos. 1-12 and 16-27), with traverse. Claims 1-27 are pending.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postpaid in an envelope, addressed to the: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on February 7, 2005.

Dated: 2/7/05



Michele Fleitman

There are two criteria for a proper requirement for restriction between patentable distinct inventions: (A) The inventions must be independent or distinct as claimed; and (B) There must be a serious burden on the Examiner if restriction is required.

Examiner stated essentially that the Group I claims, 1-12 and 16-27, are drawn to a method for hierarchical VLSI design and that the Group II claims, 13-15, are drawn to a method for processing a design graph.

The Examiner has not provided a reason and/or example to support the conclusion the groups are patentably distinct species of the claimed invention. Accordingly, no *prima facie* showing has been made to support the restriction requirement. Under such circumstances, the Examiner is encouraged to maintain all claims in the same application.

Respectfully submitted,



Nathaniel T. Wallace
Reg. No. 48,909
Attorney for Applicants

F. CHAU & ASSOCIATES, LLP
30 Woodbury Road
Woodbury, New York 11797
TEL: (516) 692-8888
FAX: (516) 692-8889